instructions to apply test vectors of the effective address pairs to a semiconductor device; and

instructions to specify a faulty part within the semiconductor device by measuring an emission from the semiconductor device.

REMARKS

Applicant's representative appreciates the courtesies extended by the Examiner during the phone interview on February 4, 2003.

By the present Amendment, Applicant amends claims 5, 9, 13, 16, and 19 pursuant to the agreement reached with the Examiner during the phone interview. In accordance with the requirements of 37 C.F.R. § 1.121(c)(1), Applicant provides a marked-up version of the amended claims in an attached Appendix. No new matter has been added by these amendments. Claims 1 - 19 remain pending.

In view of foregoing amendments and remarks, Applicant respectfully submits that pending claims 1–19 are in condition for allowance.

LAW OFFICES
FINNEGAN, HENDERSON,
FARABOW, GARRETT,
& DUNNER, L.L.P.
1300 I STREET, N. W.
WASHINGTON, DC 20005
202-408-4000

If there are any fees due under 37 C.F.R. § 114, which are not enclosed, including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge such fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: March 3, 2003

By: Richard V. Burgujian Reg 24,014
for Richard V. Burgujian
Reg. No. 31,744

LAW OFFICES
FINNEGAN, HENDERSON, FARABOW, GARRETT, & DUNNER, L.L.P.
1300 I STREET, N. W.
WASHINGTON, DC 20005
202-408-4000

ATTENTION: BOX AFTER FINAL
RESPONSE UNDER 37 C.F.R. § 1.116
EXPEDITED PROCEDURE REQUESTED
EXAMINING GROUP 2863

PATENT
Customer No. 22,852
Application No.: 09/708,490
Filed: November 9, 2000
Attorney Docket No. **3180.0269-00**

APPENDIX TO AMENDMENT OF MARCH 3, 2003
VERSION WITH MARKINGS TO SHOW CHANGES MADE

AMENDMENTS TO THE CLAIMS

Please amend claims 5, 8, 13, 16, and 19 as follows:

5. (Twice Amended) A semiconductor testing method for testing semiconductor devices, comprising:

reading measurement data of an IDDQ measuring circuit configured to test semiconductor devices by applying an effective test vector, including a test vector data and data of good samples and faulty samples returned to a manufacturer;

supplying the test vectors to the good samples and the faulty samples;

determining a range of pass/fail decision criteria and effective address pairs for testing semiconductor devices; and

applying test vectors of the effective address pairs to the semiconductor devices for testing.

9. (Twice Amended) A program with which a semiconductor testing method for testing semiconductor devices is executed by a computer in a semiconductor testing apparatus which comprises a read circuit, a determination circuit,

LAW OFFICES
FINNEGAN, HENDERSON,
FARABOW, GARRETT,
& DUNNER, L.L.P.
1300 I STREET, N. W.
WASHINGTON, DC 20005
202-408-4000

and an IDDQ measuring circuit configured to test semiconductor devices by applying an effective test vector, the program comprising:

instructions configured to read measurement data including a test vector data and data of good samples and faulty samples returned to a manufacturer;

instructions configured to supply the test vector data to good samples and faulty samples;

instructions configured to determine a range of pass/fail decision criteria and effective address pairs for testing semiconductor devices; and

instructions configured to apply test vectors of the effective address pairs for testing.

13. (Twice Amended) A semiconductor testing method of specifying a faulty part in a semiconductor device, comprising:

reading measurement data of an IDDQ measuring circuit configured to test semiconductor devices by applying an effective test vector, wherein the measurement data includes a test program, test vector data, data of good samples and faulty samples returned to a manufacturer;

supplying test vector data to good and faulty samples;

determining a range of pass/fail decision criteria and effective address pairs for testing semiconductor devices in a manufacturing process;

applying test vectors of the effective address pairs to a semiconductor device; and

LAW OFFICES
FINNEGAN, HENDERSON,
FARABOW, GARRETT,
& DUNNER, L.L.P.
1300 I STREET, N. W.
WASHINGTON, DC 20005
202-408-4000

specifying a faulty part within the semiconductor device by measuring an emission from the semiconductor device.

16. (Twice Amended) A semiconductor testing apparatus for specifying a faulty part in a semiconductor device, comprising:

a read circuit configured to read measurement data of an IDDQ measuring circuit configured to test semiconductor devices by applying an effective test vector, wherein the measurement data includes a test program, test vector data, data of good samples and faulty samples returned to a manufacturer;

a determination circuit configured to supply the test vector data to the good samples and faulty samples, and to determine a range of pass/fail decision criteria and effective address pairs for testing semiconductor devices in a manufacturing process; and

a faulty part specifying circuit configured to apply test vectors of the effective address pairs to a semiconductor device and to specify a faulty part by measuring an emission from the semiconductor device.

19. (Twice Amended) A program with which a semiconductor testing method is executed by a computer in a semiconductor testing apparatus which comprises a read circuit, a determination circuit, and a faulty part specifying circuit, the program comprising:

LAW OFFICES
FINNEGAN, HENDERSON,
FARABOW, GARRETT,
& DUNNER, L.L.P.
1300 I STREET, N. W.
WASHINGTON, DC 20005
202-408-4000

instructions configured to read measurement data of an IDDQ measuring circuit configured to test semiconductor devices by applying an effective test vector, wherein the measurement data includes a test program, test vector data, data of good samples and faulty samples returned to a manufacturer;

instructions configured to supply the test vector data to good samples and faulty samples;

instructions configured to determine a range of pass/fail decision criteria and effective address pairs for testing semiconductor devices in a manufacturing process;

instructions to apply test vectors of the effective address pairs to a semiconductor device; and

instructions to specify a faulty part within the semiconductor device by measuring an emission from the semiconductor device.

LAW OFFICES
FINNEGAN, HENDERSON,
FARABOW, GARRETT,
& DUNNER, L.L.P.
1300 I STREET, N. W.
WASHINGTON, DC 20005
202-408-4000